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EXAMINER	
LEE, CHRISTOPHER E	

ART UNIT	PAPER NUMBER
2112	

DATE MAILED: 03/15/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/767,001	ZHANG ET AL.	
	Examiner	Art Unit	
	Christopher E. Lee	2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 February 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Receipt Acknowledgement

1. Receipt is acknowledged of the Amendment filed on 27th of February 2006. Claims 19, 20, 23, and 24 have been amended; no claim has been canceled; and no claim has been newly added since the Non-Final Office Action was mailed on 20th of December 2005. Currently, claims 1-24 are pending in this Application.

Claim Objections

2. Claim 19 is objected to because of the following informalities:

Substitute "a grant indication" by --a bus grant indication-- in lines 3-4.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

5. Claims 1-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicants' Admitted Prior Art [hereinafter AAPA] in view of Park et al. [US 5,526,508 A; hereinafter Park].

Referring to claim 1, AAPA discloses a method for transferring information to a bus (i.e., Bus 106 of Fig. 1; See page 7, paragraph [0025], lines 1-3), comprising:

- receiving an indication (i.e., CPU_WR_COM or CPU_RD_COM) that information (i.e., CAD, CDW, and CCO in Figs. 2-3) is to be transferred to a bus (i.e., Bus 106 of Fig. 1; See page 8, paragraph [0028]);
- reading a bus grant indication (i.e., indication on GNT/PARKING-GNT in Fig. 2; See page 9, paragraph [0029]);
- writing the information (i.e., said CAD, CDW, and CCO) to a buffer (i.e., Two-Entry Buffer 202 of Fig. 2) if the bus grant indication does not indicate that transfer of the information to the bus is allowed (i.e., when said GNT/PARKING-GNT is not active High, said Two-Entry Buffer is holding said information CAD, CDW, and CCO); and
- transferring the information (i.e., said information CAD, CDW, and CCO in said Two-Entry Buffer) to the bus if the bus grant indication (i.e., said GNT/PARKING-GNT) indicates that transfer of the information to the bus is allowed (See page 9, paragraph [0029]).

AAPA does not teach transferring the information to the bus if the buffer is empty and the transfer of the information to the bus is allowed.

Park discloses a method for cache line replacing system (See Fig. 3 and Abstract), wherein said method (i.e., said method for cache line replacing system) for reducing latency in information transfers (See col. 3, lines 2-3) to a bus (i.e., CPU/Cache bus 31 of Fig. 3) including

- transferring an information (i.e., line of cache data) to a bus (i.e., said CPU/Cache bus) if a buffer (i.e., RD Buffer 36 of Fig. 3) is empty (i.e., said Buffer WT Reg counts 'zero'; See col. 5, lines 26-30) and transfer of the information to the bus is allowed (i.e., said CPU/Cache bus is idle after

write-back data having been stored in write-back buffer; See col. 3, lines 27-35, and col. 4, lines 31-46).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said method step of transferring, as disclosed by Park, in said method, as disclosed by AAPA, for the advantage of providing a way that a device (i.e., CPU) can read said information (i.e., data) at high speed without loss of said bus bandwidth (i.e., memory bus bandwidth; See Park, col. 6, lines 30-31).

Referring to claim 2, AAPA teaches

- the information (i.e., CAD, CDW, and CCO in Figs. 2-3) includes
  - a write command (i.e., CPU_WR_COM on CCO in Fig. 3; See page 9, paragraph [0030], lines 11-13),
  - an address (i.e., CPU_ADDR on CAD in Fig. 3; See page 9, paragraph [0030], lines 6-9), and
  - data to be written to the address (i.e., CPU_DATA_WR on CDW in Fig. 3; See page 9, paragraph [0030], lines 9-10).

Referring to claim 3, AAPA teaches

- the indication (i.e., CPU_WR_COM or CPU_RD_COM) from the device (i.e., CPU 101 of Fig. 1) that information (i.e., CAD, CDW, and CCO in Figs. 2-3) is to be transferred to the bus (i.e., Bus 106 of Fig. 1) includes
  - the write command (i.e., CPU_WR_COM on CCO in Fig. 3; See page 8, paragraph [0028], lines 6-9).

Referring to claim 4. AAPA teaches

- the information (i.e., CAD, CDW, and CCO in Figs. 2-3) includes
    - a read command (i.e., CPU_RD_COM on CCO in Fig. 4; See page 11, paragraph [0036], lines 8-10) and
    - an address from which data is to be read (i.e., CPU_ADDR on CAD in Fig. 4; See page 11, paragraph [0036], lines 5-8).

Referring to claim 5. AAPA teaches

- the indication (i.e., CPU_WR_COM or CPU_RD_COM) from the device (i.e., CPU 101 of Fig. 1) that information (i.e., CAD, CDW, and CCO in Figs. 2-3) is to be transferred to the bus (i.e., Bus 106 of Fig. 1) includes
    - the read command (i.e., CPU_RD_COM on CCO in Fig. 4; See page 8, paragraph [0028], lines 9-11).

Referring to claim 6. AAPA teaches

- access to the bus (i.e., Bus 106 of Fig. 1) is controlled by a bus arbiter (i.e., Bus Arbiter 107 of Fig. 1) employing a bus parking protocol (i.e., bus parking scheme; See PARKING_GNT in Figs. 3-4, and page 9, paragraph [0029]).

Referring to claim 7. AAPA teaches

- sending a bus access request (i.e., REQ in Fig. 2) to the bus arbiter (i.e., Bus Arbiter 107 of Fig. 1) if the bus grant indication (i.e., GNT/PARKING-GNT in Fig. 2) does not indicate that transfer of the information to the bus is allowed (i.e., Bus 106 of Fig. 1 is not available; See page 7,

paragraph [0025], lines 10-13, page 9, paragraph [0029], and page 17, paragraph [0048], lines 4-11).

Referring to claim 8, AAPA teaches

- periodically sending bus access requests (i.e., REQ in Fig. 2) to the bus arbiter (i.e., Bus Arbiter 107 of Fig. 1) and reading the bus grant indication (i.e., GNT/PARKING-GNT in Fig. 2) if the information stored in the buffer has not been transferred to the bus (See page 15, paragraph [0045], line 1 through paragraph [0046], line 12), so that when the bus grant indication indicates that transfer of the information to the bus allowed (i.e., bus is available), the information stored in the buffer is transferred to the bus (See page 2, paragraph [0004], lines 5-8).

Referring to claim 9, AAPA discloses a bus interface unit (i.e., conventional BIU 105 in Fig. 1; See page 7, paragraph [0023], lines 1-4) in information transfers from a device (i.e., CPU 101 of Fig. 1) to a bus (i.e., Bus 106 of Fig. 1; See page 7, paragraph [0025], lines 1-3), comprising:

- a buffer (i.e., Two-Entry Buffer 202 of Fig. 2) having inputs coupled to the device (i.e., said CPU; See Figs. 1-2, and page 7, paragraph [0025], lines 1-3) and
- logic (i.e., Control Logic 201 of Fig. 2) configured to
    - receive an indication (i.e., CPU_WR_COM or CPU_RD_COM) from the device (i.e., said CPU) that information (i.e., CAD, CDW, and CCO in Figs. 2-3) is to be transferred to the bus (i.e., said Bus; See page 8, paragraph [0028]),
    - read a bus grant indication (i.e., indication on GNT/PARKING-GNT in Fig. 2; See page 9, paragraph [0029]), and
    - cause the information (i.e., said CAD, CDW, and CCO) to either be stored in the buffer (i.e., said Two-Entry Buffer) if the bus grant indication does not indicate that transfer of

the information from the device (i.e., said CPU) to the bus is allowed (i.e., when said GNT/PARKING-GNT is not active High, said Two-Entry Buffer is holding said information CAD, CDW, and CCO), or be transferred from the buffer (i.e., said Two-Entry Buffer) to the bus if the bus grant indication (i.e., said GNT/PARKING-GNT) indicates that transfer of the information from the buffer to the bus is allowed (See page 9, paragraph [0029]).

AAPA does not teach said logic being configured to cause the information to be transferred from the device to the bus if the buffer is empty and the transfer of the information to the bus is allowed.

Park discloses a cache line replacement apparatus (See Fig. 3 and Abstract), wherein a bus interface unit (i.e., said cache line replacement apparatus) for reducing latency in information transfers (See col. 3, lines 2-3) from a device (i.e., Main Memory 100 of Fig. 3) to a bus (i.e., CPU/Cache bus 31 of Fig. 3) including

- logic (i.e., MUX 38 and Buffer WT Reg 37 in Fig. 3) configured to cause an information (i.e., line of cache data) to be transferred from the device (i.e., said Main Memory) to a bus (i.e., said CPU/Cache bus) if a buffer (i.e., RD Buffer 36 of Fig. 3) is empty (i.e., said Buffer WT Reg counts 'zero'; See col. 5, lines 26-30) and transfer of the information to the bus is allowed (i.e., said CPU/Cache bus is idle after write-back data having been stored in write-back buffer; See col. 3, lines 27-35, and col. 4, lines 31-46).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said logic (i.e., MUX and Buffer WT Reg), as disclosed by Park, in said logic (i.e., Control Logic), as disclosed by AAPA, for the advantage of providing a way that said device (i.e., CPU) can read said information (i.e., data) at high speed without loss of said bus bandwidth (i.e., memory bus bandwidth; See Park, col. 6, lines 30-31).

Referring to claim 10, AAPA teaches

- the information (i.e., CAD, CDW, and CCO in Figs. 2-3) includes
    - a write command (i.e., CPU_WR_COM on CCO in Fig. 3; See page 9, paragraph [0030], lines 11-13),
    - an address (i.e., CPU_ADDR on CAD in Fig. 3; See page 9, paragraph [0030], lines 6-9), and
    - data to be written to the address (i.e., CPU_DATA_WR on CDW in Fig. 3; See page 9, paragraph [0030], lines 9-10).

Referring to claim 11, AAPA teaches

- the indication (i.e., CPU_WR_COM or CPU_RD_COM) from the device (i.e., CPU 101 of Fig. 1) that information (i.e., CAD, CDW, and CCO in Figs. 2-3) is to be transferred to the bus (i.e., Bus 106 of Fig. 1) includes
    - the write command (i.e., CPU_WR_COM on CCO in Fig. 3; See page 8, paragraph [0028], lines 6-9).

Referring to claim 12, AAPA teaches

- the information (i.e., CAD, CDW, and CCO in Figs. 2-3) includes
    - a read command (i.e., CPU_RD_COM on CCO in Fig. 4; See page 11, paragraph [0036], lines 8-10) and
    - an address from which data is to be read (i.e., CPU_ADDR on CAD in Fig. 4; See page 11, paragraph [0036], lines 5-8).

Referring to claim 13, AAPA teaches

- the indication (i.e., CPU_WR_COM or CPU_RD_COM) from the device (i.e., CPU 101 of Fig. 1) that information (i.e., CAD, CDW, and CCO in Figs. 2-3) is to be transferred to the bus (i.e., Bus 106 of Fig. 1) includes
    - o the read command (i.e., CPU_RD_COM on CCO in Fig. 4; See page 8, paragraph [0028], lines 9-11).

Referring to claim 14, AAPA teaches

- access to the bus (i.e., Bus 106 of Fig. 1) is controlled by a bus arbiter (i.e., Bus Arbiter 107 of Fig. 1) employing a bus parking protocol (i.e., bus parking scheme; See PARKING_GNT in Figs. 3-4, and page 9, paragraph [0029]).

Referring to claim 15, AAPA teaches

- the logic (i.e., Control Logic 201 of Fig. 2) is further configured to send a bus access request (i.e., REQ in Fig. 2) to the bus arbiter (i.e., Bus Arbiter 107 of Fig. 1) if the bus grant indication (i.e., GNT/PARKING-GNT in Fig. 2) does not indicate that transfer of the information to the bus is allowed (i.e., Bus 106 of Fig. 1 is not available; See page 7, paragraph [0025], lines 10-13, page 9, paragraph [0029], and page 17, paragraph [0048], lines 4-11).

Referring to claim 16, AAPA teaches

- the logic (i.e., Control Logic 201 of Fig. 2) is further configured to periodically send bus access requests (i.e., REQ in Fig. 2) to the bus arbiter (i.e., Bus Arbiter 107 of Fig. 1) and read the bus grant indication (i.e., GNT/PARKING-GNT in Fig. 2) if the information stored in the buffer has not been transferred to the bus (See page 15, paragraph [0045], line 1 through paragraph [0046], line 12), so that when the bus grant indication indicates that transfer of the information to the bus

allowed (i.e., bus is available), the logic (i.e., said Control Logic) causes the information stored in the buffer is transferred to the bus (See page 2, paragraph [0004], lines 5-8).

Referring to claim 17, AAPA, as modified by Park, teaches

- the logic (i.e., Control Logic 201 in Fig. 2; AAPA, MUX 38 and Buffer WT Reg 37 in Fig. 3; Park) includes
  - a multiplexer (i.e., MUX 38 of Fig. 3; See Park, col. 4, lines 40-46) having
    - first inputs (i.e., input of said MUX being coupled to Memory Bus 32 in Fig. 3; Park) coupled to the buffer inputs (i.e., RD Buffer 36 being coupled to said Memory Bus 32 in Fig. 3; Park),
    - second inputs (i.e., input of said MUX being coupled to Bus Line 33 in Fig. 3; Park) coupled to the buffer outputs (i.e., output of said RD Buffer; Park),
    - outputs coupled to the bus (i.e., output of said MUX being coupled to CPU/Cache Bus 31 in Fig. 3; Park), and
    - at least one select input (i.e., input from said Buffer WT Reg 37 in Fig. 3; Park) for selectively coupling either the first or the second inputs to the outputs (See Park, col. 3, lines 27-35); and
- the logic (i.e., said Control Logic of AAPA, and said MUX/Buffer WT Reg of Park) is further configured to provide
  - a control output (i.e., output of said Buffer WT Reg) to the at least one select input (See Park, Fig. 3) so that the first inputs (i.e., input of said MUX being coupled to said Memory Bus of Park) are coupled to the outputs (i.e., output of said MUX being coupled to said CPU/Cache Bus of Park) if the bus grant indication (i.e., indication on GNT/PARKING-GNT in Fig. 2; See AAPA, page 9, paragraph [0029]) indicates that

transfer of the information to the bus is allowed (See AAPA, page 9, paragraph [0029], and see Park, col. 3, lines 27-35, and col. 4, lines 31-46, i.e., said CPU/Cache bus is idle after write-back data having been stored in write-back buffer) and the buffer (i.e., RD Buffer 36 of Fig. 3; Park) is empty (i.e., said Buffer WT Reg counts 'zero'; See Park, col. 5, lines 26-30).

Referring to claim 18, Park teaches

- the logic (i.e., MUX 38 and Buffer WT Reg 37 in Fig. 3) is further configured to provide
  - the control output (i.e., output of said Buffer WT Reg) to the at least one select input (See Fig. 3) so that the second inputs (i.e., input of MUX being coupled to Bus Line 33 in Fig. 3) are coupled to the outputs (i.e., output of said MUX being coupled to CPU/Cache Bus 31 in Fig. 3) if the bus grant indication does not indicate that transfer of the information to the bus (i.e., said CPU/Cache Bus) is allowed (i.e., said CPU/Cache Bus is not busy due to write-back buffering during a cache line replacing cycle, which is clearly implies the bus grant indication does not indicate that transfer of the information to the bus is allowed; See col. 4, lines 31-36).

Referring to claim 19, AAPA discloses in a computer system (i.e., in a conventional Computer System 100 in Fig. 1) including

- a bus (i.e., Bus 106 of Fig. 1) with access governed by a bus arbiter (i.e., Bus Arbiter 107 of Fig. 1) employing a bus parking scheme (See PARKING_GNT in Figs. 3-4, and page 9, paragraph [0029]) and
- a buffer (i.e., Two-Entry Buffer 202 of Fig. 2) having inputs coupled to a device (i.e., CPU 101 of Fig. 1) so that

- information (i.e., CAD, CDW, and CCO in Figs. 2-3) to be transferred from the device to the bus (See page 7, paragraph [0025], lines 1-3) is stored in the buffer if a bus grant indication (i.e., indication on GNT/PARKING-GNT in Fig. 2) generated by the bus arbiter (See page 9, paragraph [0029]) indicates that the bus is unavailable for the transfer (i.e., when said GNT/PARKING-GNT is not active High, said Two-Entry Buffer is holding said information CAD, CDW, and CCO in Figs. 2-3), or the bus grant indication (i.e., said indication on GNT/PARKING-GNT) indicates that the bus is available for transfer of the information to the bus (i.e., indicating that transfer of the information to the bus is allowed; See page 9, paragraph [0029]).

AAPA does not teach a buffer bypass circuit for reducing latency in information transfers to the bus comprising: a multiplexer having first inputs coupled to inputs to the buffer, second inputs coupled to outputs of the buffer, outputs coupled to the bus, and at least one select input for selectively coupling either the first or the second inputs to the outputs; and logic configured to provide control information to the at least one select input such that the first inputs are coupled to the outputs of the multiplexer if the buffer is empty and the bus is available for transfer of the information to the bus.

Park discloses a cache line replacement apparatus (See Fig. 3 and Abstract), wherein a buffer bypass circuit (i.e., said cache line replacement apparatus) for reducing latency in information transfers (See col. 3, lines 2-3) to a bus (i.e., CPU/Cache bus 31 of Fig. 3) comprising:

- a multiplexer (i.e., MUX 38 of Fig. 3; See col. 4, lines 40-46) having
  - first inputs (i.e., input of said MUX being coupled to Memory Bus 32 in Fig. 3) coupled to inputs to a buffer (i.e., RD Buffer 36 being coupled to said Memory Bus 32 in Fig. 3),
  - second inputs (i.e., input of said MUX being coupled to Bus Line 33 in Fig. 3) coupled to outputs of the buffer (i.e., output of said RD Buffer),

- outputs coupled to the bus (i.e., output of said MUX being coupled to CPU/Cache Bus 31 in Fig. 3), and
- at least one select input (i.e., input from Buffer WT Reg 37 in Fig. 3) for selectively coupling either the first or the second inputs to the outputs (See col. 3, lines 27-35); and

- logic (i.e., MUX 38 and Buffer WT Reg 37 in Fig. 3) configured to provide
  - control information (i.e., MUX control information from said Buffer WT Reg) to the at least one select input (i.e., input of said MUX being coupled to said Memory Bus) such that the first inputs (i.e., input of said MUX being coupled to said Memory Bus) are coupled to the outputs of the multiplexer (i.e., output of said MUX being coupled to said CPU/Cache Bus) if the buffer (i.e., said RD Buffer) is empty (i.e., said Buffer WT Reg counts 'zero'; See col. 5, lines 26-30) and the bus is available for transfer of the information to the bus (i.e., said CPU/Cache bus is idle after write-back data having been stored in write-back buffer; See col. 3, lines 27-35, and col. 4, lines 31-46).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said buffer bypass circuit, as disclosed by Park, in said logic (i.e., Control Logic), as disclosed by AAPA, for the advantage of providing a way that said device (i.e., CPU) can read said information (i.e., data) at high speed without loss of said bus bandwidth (i.e., memory bus bandwidth; See Park, col. 6, lines 30-31).

Referring to claim 20, AAPA, as modified by Park, teaches

- the logic (i.e., Control Logic 201 in Fig. 2; AAPA, MUX 38 and Buffer WT Reg 37 in Fig. 3; Park) is further configured to provide
  - control information (i.e., MUX control information from said Buffer WT Reg; Park) to the at least one select input (i.e., input of said MUX being coupled to said Memory Bus; Park)

generated such that after checking the bus grant indication (i.e., checking GNT/PARKING-GNT in Fig. 2; See AAPA, page 9, paragraph [0029]) the second inputs (i.e., input of MUX being coupled to Bus Line 33 in Fig. 3; Park) are coupled to the outputs of the multiplexer (i.e., output of said MUX being coupled to CPU/Cache Bus 31 in Fig. 3; Park) if the buffer (i.e., RD Buffer 36 of Fig. 3; Park) is not empty (See Park, col. 3, lines 27-32 and col. 4, lines 40-44) and the bus grant indication indicates that the bus is available for transfer of the information to the bus (See AAPA, page 9, paragraph [0029], lines 9-13), or the bus grant indication does not indicate that the bus is available for transfer of the information to the bus (i.e., when said GNT/PARKING-GNT is not active High, said Two-Entry Buffer is holding said information CAD, CDW, and CCO; AAPA, and Park suggests the input of MUX being coupled to said Bus Line is still connected to the outputs of the multiplexer as long as the count value of said Buffer WT Reg is larger than zero; See Park, col. 4, lines 42-44).

Referring to claim 21, AAPA teaches

- the information (i.e., CAD, CDW, and CCO in Figs. 2-3) includes
  - a write command (i.e., CPU_WR_COM on CCO in Fig. 3; See page 9, paragraph [0030], lines 11-13),
  - an address (i.e., CPU_ADDR on CAD in Fig. 3; See page 9, paragraph [0030], lines 6-9), and
  - data to be written to the address (i.e., CPU_DATA_WR on CDW in Fig. 3; See page 9, paragraph [0030], lines 9-10).

Referring to claim 22, AAPA teaches

- the information (i.e., CAD, CDW, and CCO in Figs. 2-3) includes

- a read command (i.e., CPU_RD_COM on CCO in Fig. 4; See page 11, paragraph [0036], lines 8-10) and
- an address from which data is to be read (i.e., CPU_ADDR on CAD in Fig. 4; See page 11, paragraph [0036], lines 5-8).

Referring to claim 23, AAPA teaches

- the logic (i.e., Control Logic 201 of Fig. 2) is further configured to send a bus access request (i.e., REQ in Fig. 2) to the bus arbiter (i.e., Bus Arbiter 107 of Fig. 1) if the bus grant indication (i.e., GNT/PARKING-GNT in Fig. 2) does not indicate that the bus is available for transfer of the information to the bus (i.e., Bus 106 of Fig. 1 is not available; See page 7, paragraph [0025], lines 10-13, page 9, paragraph [0029], and page 17, paragraph [0048], lines 4-11).

Referring to claim 24, AAPA teaches

- the logic (i.e., Control Logic 201 of Fig. 2) is further configured to periodically send bus access requests (i.e., REQ in Fig. 2) to the bus arbiter (i.e., Bus Arbiter 107 of Fig. 1) and read the bus grant indication (i.e., GNT/PARKING-GNT in Fig. 2) if the information stored in the buffer has not been transferred to the bus (See page 15, paragraph [0045], line 1 through paragraph [0046], line 12), so that when the grant indication indicates that the bus is available for transfer of the information to the bus (i.e., bus is allowed to transfer), the information stored in the buffer is transferred to the bus (See page 2, paragraph [0004], lines 5-8).

Response to Arguments

6. Applicant's arguments filed on 27th of February 2006 have been fully considered but they are not persuasive.

In response to the Applicants' argument with respect to "... Park et al. does not describe the use of a bus grant indication to determine if the transfer of information to the bus is allowed. The Office states that Park describes transferring information to a bus if a buffer is empty and the transfer of the information to the bus is allowed. To support this statement, the Office states that Park describes the CPU/cache bus as being idle after the write-back data has been stored in the write-back buffer, at col. 3, lines 27-35, and col. 4, lines 31-46. Applicants respectfully disagree with the Office regarding this finding. Park does not describe the bus as being idle after the write-back process is completed. In fact, with reference col. 4, lines 31-36 of Park, the data stored in the read buffer 36 is stored during the time when the write-back data is being stored in the write-back buffer 35. Then, immediately after the storage of the write-back data is completed, the data of the read buffer 35 is transmitted to the CPU/cache bus 31 through multiplexer 38. As described by Park at col. 4, lines 45-47, the multiplexer 38 continuously transmits the data of memory bus 32 to the CPU/cache bus 31 when the value of register 37 becomes zero. Clearly, Park does not describe a step for the determination of whether or not the CPU/cache bus 31 is available for transfer, but rather that the data is continuously transmitted regardless of the status of the CPU/cache bus 31. Additionally, Park does not employ a bus grant indication or any other form of indication as to whether or not the bus is available for transfer. To establish a *prima facie* case of obviousness, ..." in the Response page 10, the Examiner respectfully disagrees.

Park discloses a cache line replacing system (See Abstract and Figs. 3 and 5) for reducing latency in transferring line of cache data (See col. 3, lines 2-3) to a CPU/Cache bus, wherein transferring a line of cache data (i.e., information) to a CPU/Cache bus if a RD Buffer is empty (i.e., said Buffer WT Reg counts 'zero'; See col. 5, lines 26-30) and transferring said line of cache data to said CPU/Cache bus is allowed, i.e., said CPU/Cache bus is idle after write-back data having been stored in write-back buffer (viz., after storage of write-back data being completed, and then before reading data from read buffer into said CPU/cache bus, which is the allowing time of transferring said line of cache data to said CPU/Cache

bus; See Fig. 5, Step 52, if the condition is 'Y', then said CPU/Cache bus is available to be used (viz., bus idle) for transferring read data into CPU/Cache). In other words, memory read data is directly transferred from main memory to CPU/Cache bus without using RD Buffer (i.e., bypassing buffer) if said RD Buffer is empty and said CPU/cache bus is available to be used (viz., bus idle) for transferring read data into CPU/cache (i.e., allowed).

In particular, Park clearly suggests the bus (i.e., CPU/Cache bus) as being idle after the write-back process is completed (i.e., as being available to transfer data from RD Buffer or main memory to said CPU/cache bus after the write-back process is completed; in fact, said CPU/cache bus is idle after the write-back process is completed), which is in contrary to the Applicants' argument.

And, further, Park describes that the read data is transmitted with regard to the status of the CPU/Cache bus. In other words, if said CPU/Cache bus is used by write-back data process (i.e., bus busy), the read data is buffered in the RD Buffer until said CPU/Cache bus is available, and if storage of write-back data is completed (i.e., implying bus status changing from bus busy to bus idle), the read data is transferred from the RD Buffer to said CPU/Cache bus or said CPU/Cache bus is in idle until the read data is retrieved from the main memory and directly transferred to said CPU/Cache bus (See Fig. 5 and col. 6, lines 9-24).

Even though the Applicants allege that the data of the RD buffer is immediately transmitted to the CPU/Cache bus through multiplexer after the storage of the write-back data is completed, it would be one of particular examples. In other words, no data might be immediately transmitted to said CPU/Cache bus after the storage of the write-back data is completed if said RD Buffer is empty, or the read data is directly transferred from main memory to said CPU/Cache bus (i.e., bypassing buffer) when said CPU/Cache bus is available to be used, i.e., bus idle status, and the RD buffer is empty. Therefore, Park clearly suggests the claimed limitation "transferring the information to the bus if the buffer is empty and the transfer of the information to the bus is allowed."

Furthermore, the Applicants argue that Park does not employ a bus grant indication or any other form of indication as to whether or not the bus is available for transfer. However, the primary reference AAPA teaches the above argued limitation on page 9, paragraph [0029]. And, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

Therefore, the combination of AAPA and Park with rationale for proper combination clearly suggests the obviousness of the claimed invention (See paragraph 5 of the instant Office Action, claims 1-24 rejection under 35 U.S.C. 103(a) as being unpatentable over AAPA in view of Park), and thus the Applicants' arguments on these points are not persuasive.

In response to the Applicants' argument with respect to "... Applicants respectfully disagree with the finding of the Office. Park does not describe logic configured to cause information to be transferred from the device to the bus if the buffer is empty and the bus grant indication indicates that transfer of the information to the bus is allowed. .:. Clearly, Park does not describe logic configured to cause information to be transferred from the device "to the bus if the buffer is empty and the bus grant indication indicates that transfer of the information to the bus is allowed," as is recited in claim 9. Rather, Park describes the data as being continuously transmitted regardless of the status of the CPU/cache bus 31. To establish a *prima facie* case of obviousness, ..." in the Response page 11, lines 1-23, the Examiner respectfully disagrees.

As is stated above response, Park discloses a cache line replacing system (See Abstract and Figs. 3 and 5) for reducing latency in transferring line of cache data (See col. 3, lines 2-3) to a CPU/Cache bus, wherein MUX and Buffer WT Reg (i.e., logic) configured to cause a line of cache data (i.e., information) to be transferred from main memory (i.e., device) to CPU/Cache bus if a RD Buffer is empty (i.e., said Buffer WT Reg counts 'zero'; See col. 5, lines 26-30) and transferring said line of cache data to said

CPU/Cache bus is allowed, i.e., said CPU/Cache bus is idle after write-back data having been stored in write-back buffer (viz., after storage of write-back data being completed, and then before reading data from read buffer into said CPU/cache bus, which is the allowing time of transferring said line of cache data to said CPU/Cache; See Fig. 5, Step 52, if the condition is 'Y', then said CPU/Cache bus is available to be used (viz., bus idle) for transferring read data into CPU/Cache).

And, in contrary to the Applicants' assertion, i.e., Park describes the data as being continuously transmitted regardless of the status of the CPU/Cache bus, Park discloses that the read data is transmitted with regard to the status of the CPU/Cache bus. In other words, if said CPU/Cache bus is used by write-back data process (i.e., bus busy), the read data is buffered in the RD Buffer until said CPU/Cache bus is available, and if storage of write-back data is completed (i.e., implying bus status changing from bus busy to bus idle), the read data is transferred from the RD Buffer to said CPU/Cache bus or said CPU/Cache bus is in idle until the read data is retrieved from the main memory and directly transferred to said CPU/Cache bus (See Fig. 5 and col. 6, lines 9-24).

Therefore, the combination of AAPA and Park with rationale for proper combination clearly suggests the obviousness of the claimed invention (See paragraph 5 of the instant Office Action, claims 1-24 rejection under 35 U.S.C. 103(a) as being unpatentable over AAPA in view of Park).

Furthermore, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

Thus the Applicants' arguments on these points are not persuasive.

In response to the Applicants' argument with respect to "... Applicants respectfully disagree with the finding of the Office. Park does not describe logic configured to provide control information to the at least one select input such that the first inputs are coupled to the outputs of the multiplexer if the buffer is empty and the bus grant indication indicates that the bus is available for transfer of the information to the

bus. ... Clearly, Park does not describe "to provide control information to the at least one select input such that the first inputs are coupled to the outputs of the multiplexer if the buffer is empty and the bus grant indication indicates that the bus is available for transfer of the information to the bus," as is recited in claim 19. Rather, Park describes the data as being continuously transmitted regardless of the status of the CPU/cache bus 31. Additionally, Park does not employ a bus grant indication or any other form of indication as to whether or not the bus is available for transfer. To establish a *prima facie* case of obviousness, ..." in the Response page 11, line 24 through page 12, line 25, the Examiner respectfully disagrees.

As is stated above response, Park discloses a cache line replacing system (See Abstract and Figs. 3 and 5) for reducing latency in transferring line of cache data (See col. 3, lines 2-3) to a CPU/Cache bus, wherein MUX and Buffer WT Reg (i.e., logic) configured to provide MUX control information from said Buffer WT Reg (i.e., control information) to the at least one select input of said MUX being coupled to said Memory Bus such that the first inputs of said MUX being coupled to said Memory Bus are coupled to the outputs said MUX being coupled to said CPU/Cache bus if the RD Buffer is empty (i.e., said Buffer WT Reg counts 'zero'; See col. 5, lines 26-30) and the CPU/Cache bus is available for transferring line of cache data to the CPU/Cache bus, i.e., said CPU/Cache bus is idle after write-back data having been stored in write-back buffer (viz., after storage of write-back data being completed, and then before reading data from read buffer into said CPU/cache bus, which is the allowing time of transferring said line of cache data to said CPU/Cache bus; See Fig. 5, Step 52, if the condition is 'Y', then said CPU/Cache bus is available to be used (viz., bus idle) for transferring read data into CPU/Cache).

And, in contrary to the Applicants' assertion, i.e., Park describes the data as being continuously transmitted regardless of the status of the CPU/Cache bus, Park discloses that the read data is transmitted with regard to the status of the CPU/Cache bus. In other words, if said CPU/Cache bus is used by write-back data process (i.e., bus busy), the read data is buffered in the RD Buffer until said CPU/Cache bus is

available, and if storage of write-back data is completed (i.e., implying bus status changing from bus busy to bus idle), the read data is transferred from the RD Buffer to said CPU/Cache bus or said CPU/Cache bus is in idle until the read data is retrieved from the main memory and directly transferred to said CPU/Cache bus (See Fig. 5 and col. 6, lines 9-24).

Furthermore, the Applicants argue that Park does not employ a bus grant indication or any other form of indication as to whether or not the bus is available for transfer. However, the primary reference AAPA teaches the above argued limitation on page 9, paragraph [0029]. And, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

Therefore, the combination of AAPA and Park with rationale for proper combination clearly suggests the obviousness of the claimed invention (See paragraph 5 of the instant Office Action, claims 1-24 rejection under 35 U.S.C. 103(a) as being unpatentable over AAPA in view of Park).

Thus the Applicants' arguments on these points are not persuasive.

Conclusion

7. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christopher E. Lee whose telephone number is 571-272-3637. The examiner can normally be reached on 9:30am - 5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rehana Perveen can be reached on 571-272-3676. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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CEL/

Christopher E. Lee